Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented): A ball grid array package semiconductor device, the device being supplied with two or more external powers including a first power and a second power, the device comprising:

a semiconductor chip having a plurality of pads arranged along a first surface thereof;

a substrate having a first surface which confronts the first surface of the semiconductor chip and an opposite second surface, the substrate further having a slot extending there through which is aligned over the plurality of pads to expose the plurality of pads;

a bonding material inserted between the respective first surfaces of the semiconductor chip and the substrate to fix the semiconductor chip to the substrate;

a first rectangular signal line plane having a first rectangular surface area ~~of~~ located over the second surface of the substrate on one side of the slot;

a second rectangular signal line plane having a second rectangular surface area located over the second surface of the substrate on another side of the slot;

a first plurality ball mounts located within the first rectangular surface area of the first rectangular signal line plane;

a second plurality of ball mounts located within the second rectangular surface area of the second rectangular signal line plane;

a first plurality of balls respectively mounted within the first plurality of ball mounts, wherein some of the first plurality of balls are electrically connected to the first rectangular signal line plane and others of the first plurality of balls are electrically isolated from the first rectangular signal line plane;

a second plurality of balls respectively mounted within the second plurality of ball mounts, wherein some of the second plurality of balls are electrical connected to the second rectangular signal line plane and others of the second plurality of balls are electrically isolated from the second rectangular signal line plane; and

a plurality of wirings for connecting the first and second rectangular signal planes and at least some of the first and second plurality of balls to respective pads of the semiconductor chip through the slot;

wherein the first power is applied to at least one of the first plurality of balls which is electrically connected to the first rectangular signal line plane, and wherein the second power is applied to at least one of the second plurality of balls which is connected to the second rectangular signal line plane.

2. (previously presented): The ball grid array package semiconductor device of claim 1, wherein the lines for the first power are combined with each other on the first rectangular signal line plane, thereby forming a first combined plane exhibiting a single node electrically, and the lines for the second power are combined with each other on the second rectangular signal line plane, thereby forming second combined plane exhibiting a single node electrically.

3. (original): The ball grid array package semiconductor device of claim 1, wherein the device is a chip scale package semiconductor device.

4. (original): The ball grid array package semiconductor device of claim 1, wherein the first power has a positive voltage and the second power is ground.

5. (withdrawn): The ball grid array package semiconductor device of claim 4, wherein the semiconductor chip comprises a triple-well structure having a P-substrate, the first power is applied to an N-well of the semiconductor chip, and the second power is applied to the P-substrate and a pocket P-well of the semiconductor chip.

6. (withdrawn): The ball grid array package semiconductor device of claim 4, wherein the semiconductor chip comprises a triple-well structure having a P-substrate, the first power is applied to an N-well of the semiconductor chip, and the second power is applied to one of the P-substrate and a pocket P-well of the semiconductor chip.

7. (withdrawn): The ball grid array package semiconductor device of claim 4, wherein the semiconductor chip comprises a twin-well structure, the first power is applied to an N-well of the semiconductor chip, and the second power is applied to a P-substrate of the semiconductor chip.

8. (withdrawn): A ball grid array package semiconductor device, the device being supplied with two or more external powers, the device comprising:

a semiconductor chip having a pad at its center of a surface thereof;

a substrate having a slot of a predetermined size and centrally arranged in a spaced relationship to the pad, the substrate having a signal line plane including a signal line pattern and a plurality of ball mounts on its one side, and wherein the semiconductor chip is mounted on an other side thereof;

a bonding material inserted between the semiconductor chip and the substrate to fix the semiconductor chip to the substrate; and

a plurality of balls mounted on the plurality of ball mounts to be connected to an external circuit,

wherein the signal line plane is divided into a plurality of signal line planes, and lines for at least one selected power among the external powers are formed only on a corresponding signal line plane.

9. (withdrawn): The ball grid array package semiconductor device of claim 8, wherein the lines for the at least one selected power among the external powers are combined with each other on the corresponding signal line plane, thereby forming a combined plane exhibiting a single node electrically.

10. (withdrawn): The ball grid array package semiconductor device of claim 8, wherein the device is a chip scale package semiconductor device.

11. (previously presented): A ball grid array package semiconductor device having a plurality of balls, including a plurality of power balls and a plurality of ground balls, the ball grid array package semiconductor device comprising:

a semiconductor chip comprising a plurality of pads, including a plurality of power pads and a plurality of ground pads, arranged along a first surface thereof; and

a single layer substrate having a first surface which confronts the first surface of the semiconductor chip and an opposite second surface, the substrate further including a slot extending there through which is aligned over the plurality of pads to expose the plurality of pads;

a rectangular power plane having a first rectangular surface area located over the second surface of the substrate on one side of the slot, the power plane including power ball mounts, power balls and the power pads;

a rectangular ground plane having a second rectangular surface area located over the second surface of the substrate on another side of the slot, the ground plane including ground ball mounts, ground balls and the ground pads; and

a plurality of signal ball mounts located within and electrically isolated from at least one of the first and second rectangular surface areas of the rectangular power plane and the rectangular ground plane, respectively;

wherein the semiconductor chip is mounted to the first side of the substrate such that the plurality of pads are electrically connected to the power ball mounts, the ground ball mounts and the signal ball mounts.

12. (previously presented): The ball grid array package semiconductor device of claim 11, wherein a boundary defining the rectangular power plane wraps around signal ball mounts positioned on the power plane and their interconnection lines.

13. (previously presented): The ball grid array package semiconductor device of claim 11, wherein a boundary defining the rectangular ground plane

wraps around signal ball mounts positioned on the ground plane and their interconnection lines.

14. (previously presented): The ball grid array package semiconductor device of claim 11, further comprising a power ball mount separated from the rectangular power plane and connected to an external circuit.

15. (previously presented): The ball grid array package semiconductor device of claim 11, further comprising a ground ball mount separated from the rectangular ground plane and connected to an external circuit.